at least one of the selecting switch sections comprise:

a buffer section for receiving delayed input signal from one of the delay stages; and

a selecting section directly connected to the buffer section for activating the buffer section to establish the delay path, and wherein

an output signal from the delay path has a desired delay time.

2. (Amended) The delay circuit according to claim 1, wherein at least one of the predetermined delay stages is provided with an individual delayed output terminal for outputting an individual delayed output signal having an individual predetermined delay time, and wherein at least one selecting switch section is provided for each individual delayed output terminal with an input terminal of the buffer section being connected to the individual delayed output terminal and output terminals of the selecting switch sections being mutually joined.

3. (Amended) The delay circuit according to claim 1, wherein at least one predetermined delay stage is provided with an individual delay input terminal for inputting a signal to which the predetermined delay time is added, the rise delay time and fall delay time for the signal inputted to each of the predetermined delay stages are substantially uniform, and wherein at least one selecting switch section is provided for each individual delay input terminal with an output terminal of the selecting switch section being connected to the individual delay input terminal and input terminals of the buffer sections being mutually joined.

4. (Amended) The delay circuit according to claim 1, wherein, the buffer section is provided with a first transistor whose gate terminal is set as an input terminal,

and the selecting section is provided with a second transistor into whose gate terminal a control signal for establishing the delay path in the delay section is input, and the first and second transistors are connected directly in series between the output terminal of the selecting switch section and a first power supply voltage.

5. (Amended) The delay circuit according to claim 4, wherein the first transistor is connected between the second transistor and the output terminal.

6. (Amended) The delay circuit according to claim 4, wherein the first transistor is connected between the second transistor and the first power supply voltage.

7. (Amended) The delay circuit according to claim 4, wherein the buffer section further comprises a third transistor whose gate terminal is connected to the input terminal, and the selecting section further comprises a fourth transistor into whose gate terminal the control signal for establishing the delay path in the delay section is input, and the third and fourth transistors are connected directly in series between the output terminal of the selecting switch section and a second power supply voltage.

8. (Amended) The delay circuit according to claim 7, wherein the first transistor is connected between the second transistor and the output terminal of the selecting switch section and the third transistor is connected between the fourth transistor and the output terminal.

9. (Amended) The delay circuit according to claim 7, wherein the second transistor is connected between the first transistor and the output terminal of the selecting switch section and the fourth transistor is connected between the third transistor and the output terminal.

14. (Amended) The delay circuit according to claim 4, wherein drive capacity of the second transistor is larger than drive capacity of the first transistor.

15. (Amended) The delay circuit according to claim 7, wherein drive capacity of the fourth transistor is larger than drive capacity of the third transistor.

16. (Amended) The delay circuit according to claim 2, wherein, in the delay section, the individual delayed output terminal is connected to an input terminal of the next one of the predetermined delay stages and a plurality of the predetermined delay stages are connected in series.

17. (Amended) The delay circuit according to claim 3, wherein, in the delay section, the output terminal of each of the predetermined delay stages is connected to the individual delayed input terminal of the next one of the predetermined delay stages and a plurality of the predetermined delay stages are connected in series.

18. (Amended) The delay circuit according to claim 16, wherein, in at least one of the predetermined delay stages, the rise delay time and fall delay time for a signal inputted to each of the predetermined delay stages are substantially uniform.

19. (Amended) The delay circuit according to claim 18, wherein each of the predetermined delay stages comprise an even number of logic inversion sections connected in series, in which the rise delay time and fall delay time for the signal are substantially uniform.

21. (Amended) The delay circuit according to claim 16, wherein each of the predetermined delay stage comprises an even number of logic inversion sections

connected in series, in which the rise delay time and fall delay time of the signal are different.

22. (Amended) The delay circuit according to claim 21, wherein each of the logic inversion sections is a NAND gate that forms inverted logic through input terminals other than the input terminal into which the signal is input being connected to a power supply voltage potential.

23. (Amended) The delay circuit according to claim 21, wherein each of the logic inversion sections is a NOR gate that forms inverted logic through input terminals other than the input terminal into which the signal is input being connected to a ground potential.

25. (Amended) The delay circuit according to claim 4, wherein, when the delay path in the delay section is established using two or more control signals, there is provided instead of the second transistor, two or more transistors connected in series into whose respective gate terminals the respective control signals are input.

26. (Amended) A semiconductor integrated circuit device comprising:

a delay section having two or more predetermined delay stages, each predetermined delay stage adds a predetermined delay time to an input signal; and

selecting switch sections for establishing a delay path for the input signal by selecting one of the selecting switch sections, wherein at least one of the selecting switch sections comprise:

a buffer section for receiving delayed input signal from one of the delay stages; and

a selecting section directly connected to the buffer section for activating the buffer section to establish the delay path, and wherein an output signal from the delay path has a desired delay time.

27. (Amended) The semiconductor integrated circuit device according to claim 26, wherein, the buffer section is provided with a first transistor whose gate terminal is set as an input terminal, and the selecting section is provided with a second transistor into whose gate a terminal control signal for establishing the delay path in the delay section is input, and the first and second transistors are connected directly in series between the output terminal of the selecting switch section and a first power supply voltage.

28. (Amended) The semiconductor integrated circuit device according to claim 26, wherein, in at least one of the predetermined delay stages, the rise delay time and fall delay time for a signal inputted to each of the predetermined delay stages are substantially uniform.

29. (Amended) A delay method comprising:

a delay step in which predetermined delay times are sequentially added onto an input signal to obtain delay signals;

a selecting step which is activated only when one of the delay signals in the delay step has a desired delay time; and

an output step in which one of the delay signals in the delay step is output by activating the selecting step.